CLAIMS

1. A semiconductor device comprising:

a gate electrode formed on a semiconductor substrate through a gate insulating film;

a pair of impurity diffusion layers formed on the surface region of said semiconductor substrate at both sides of said gate electrode; and

a first insulating film formed so as to cover the sidewalls of said gate electrode, and to extend to the surface area of said semiconductor substrate in the vicinity of said gate electrode.

2. The semiconductor device according to claim 1, wherein said first insulating film is formed in a substantially uniform thickness.

3. The semiconductor device according to claim 1, further comprising a second insulating film that covers said first insulating film and said semiconductor substrate including said gate electrode, and functions as an etch-stopper film.

4. The semiconductor device according to claim 1, wherein the lateral length of said first insulating film is twice the thickness of said first insulating film or more at the side of said gate electrode.

5. The semiconductor device according to claim 3, wherein the thickness of said second insulating film on the sidewall of

said gate electrode is smaller than the thickness of said second insulating film on the top surface of said gate electrode, and the thickness of said second insulating film on the sidewall of said gate electrode is smaller than the thickness of said second insulating film on the surface of said semiconductor substrate.

6. The semiconductor device according to claim 3, wherein the thickness of said second insulating film on the top surface of said gate electrode is smaller than the thickness of said second insulating film on the surface of said semiconductor substrate.

7. The semiconductor device according to claim 1, wherein the sum of the thickness of said first insulating film and the thickness of said second insulating film on the sidewall of said gate electrode is substantially equal to the lateral length of said first insulating film at the side of said gate electrode.

8. The semiconductor device according to claim 1, further comprising an interlayer insulating film formed between said gate electrodes adjacent to each other, and a hollow region is formed in said interlayer insulating film between said gate electrodes.

9. The semiconductor device according to claim 1, further comprising a low-resistance film on the side of said gate electrode.

10. The semiconductor device according to claim 1, further comprising an interlayer insulating film formed between said gate electrodes adjacent to each other, and a film that has a low specific

inductive capacity at least lower than the specific inductive capacity of a silicon oxide film, said film being formed on said interlayer insulating film and said gate electrode.

11. The semiconductor device according to claim 1, further comprising a contact electrode connected to said gate electrode on said gate electrode, and connected to one of said impurity diffusion layers.

12. A method for manufacturing a semiconductor device comprising:

a first step of forming a gate electrode on a semiconductor substrate through a gate insulating film;

a second step of forming a first insulating film so as to cover the top surface and the sides of said gate electrode, and the surface said semiconductor substrate;

a third step of forming an etching mask film for etching said first insulating film on said first insulating film;

a fourth step of removing said etching mask film except from the side of said gate electrode by anisotropic etching, and removing said first insulating film by continuing the etching using said etching mask film remaining on the sidewalls of said gate electrode as the mask, to make said first insulating film has a configuration to extend from said sidewalls of said gate electrode to the surface area of said semiconductor substrate underneath said remaining etching mask film;

a fifth step of removing said etching mask film; and

a sixth step of forming a second insulating film on the surface of said semiconductor substrate, so as to cover said gate electrode and said semiconductor substrate.

13. The method for manufacturing a semiconductor device according to claim 12, wherein etching in said fourth step is performed so that the lateral length of said first insulating film on said semiconductor substrate becomes twice the thickness of said first insulating film or more at the side of said gate electrode.

14. The method for manufacturing a semiconductor device according to claim 12, wherein said second insulating film is formed in said sixth step, so that the thickness of said second insulating film on the sidewalls of said gate electrode is smaller than the thickness of said second insulating film on the top surface of said gate electrode, and the thickness of said second insulating film on the sidewalls of said gate electrode is smaller than the thickness of said second insulating film on the surface of said semiconductor substrate.

15. The method for manufacturing a semiconductor device according to claim 12, wherein said second insulating film is formed in said sixth step, so that the thickness of said second insulating film on the top surface of said gate electrode is smaller

than the thickness of said second insulating film on the surface of said semiconductor substrate.

16. The method for manufacturing a semiconductor device according to claim 12, wherein said first and second insulating films are formed so that the sum of the thickness of said first insulating film and the thickness of said second insulating film on the sidewall of said gate electrode is substantially equal to the lateral length of said first insulating film at the side of said gate electrode on said semiconductor substrate.

17. The method for manufacturing a semiconductor device according to claim 12, further comprising after said fourth step,

a seventh step of forming the impurity diffusion layer on the surface of said semiconductor substrate at the side of gate electrode by ion implantation,

a eightth step of forming a refractory metal film on said gate electrode and said impurity diffusion layer, and

a ninth step of forming a low-resistance film by allowing said refractory metal film to be subjected to heat treatment to react with said gate electrode, or said impurity diffusion layer of said semiconductor substrate.

18. The method for manufacturing a semiconductor device according to claim 12, further comprising after said fourth step,

a tenth step of forming a pair of impurity diffusion layer on the surface of said semiconductor substrate at the side of gate electrode, and further comprising after said sixth step:

an eleventh step of forming an interlayer insulating film on said second insulating film;

a twelfth step of forming an opening that reaches said impurity diffusion layer in said interlayer insulating film and said second insulating film; and

a thirteenth step of forming a conductive film that fills said opening,

wherein in said twelfth step, said opening is formed so as to reach said gate electrode as well as one of said pair of impurity diffusion layers, and

in said thirteenth step, said conductive film is connected to said gate electrodes and said one of impurity diffusion layer.

19. The method for manufacturing a semiconductor device according to claim 18, further comprising after said eleventh step:

a fourteenth step of forming a hollow region in said interlayer insulating film between said gate electrodes adjacent to each other.

20. The method for manufacturing a semiconductor device according to claim 12, further comprising after said sixth step;

a fifteenth step of forming an interlayer insulating film on said second insulating film;

a sixteenth step of polishing and removing said interlayer insulating film and said second insulating film on said gate electrode until the top surface of said gate electrode is exposed; and

a seventeenth step of forming a film that has a low specific inductive capacity at least lower than the specific inductive capacity of a silicon oxide film on said exposed gate electrode, and said semiconductor substrate including the area on said interlayer insulating film between said gate electrodes.